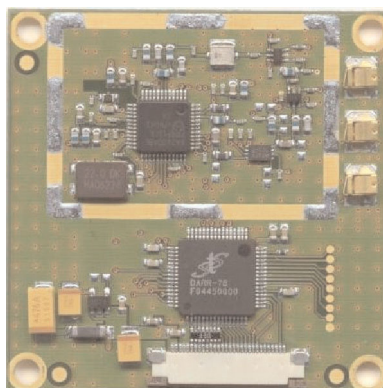


MAXII Wireless Audio Platform

Hardware Development DWAM78/DARR78



This document addresses some of the issues involved with application hardware development using the DWAM78 Digital Wireless Audio Module (B2400-GAP) or the DARR78 Digital Audio Baseband Processor.

The SW development is briefly described in a separate document.

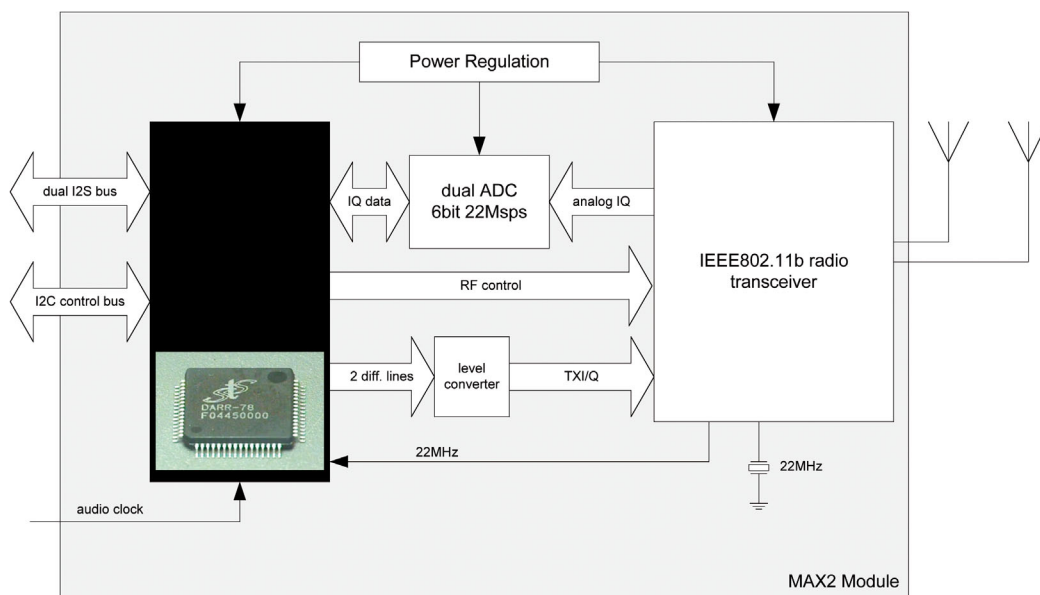
HW Development using DARR78

When the agreed business model calls for the development and/or manufacturing of a DARR78 based design being at the customer's control, STS can make available reference designs, gerber file PCB data and production documents to enable a stream lined development flow and a quick production start.

For a quick overview, the reader is referred to the "HW Development using DWAM78" section here below describing the periphery. The core of the technology, the DWAM78 itself, can be easily understood by considering the following simplified block diagram:



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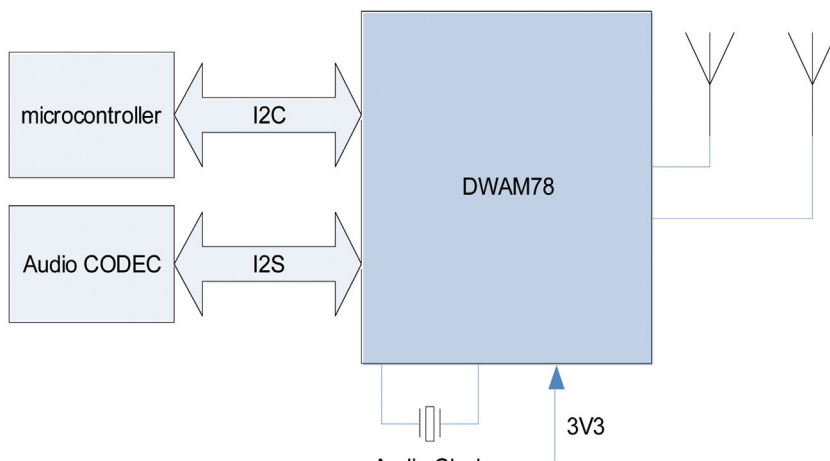
In short, the wireless part consists of an ADC, an IEEE802.11b radio transceiver and the DARR78 baseband processor. As will be explained in the section here below, the periphery consists of an audio CODEC and a microcontroller.

It is beyond the scope of this document to describe all relevant schematics and layout considerations. For more detailed information, the reader is requested to contact info@sts.nl.

Short description DWAM78

Simply said, the DWAM78 is a digital audio (I2S) to RF converter (and vice versa). It needs to be configured to the application of choice through the I2C control bus. After configuration, it can accept or output an I2S data stream that can be connected directly to an audio CODEC without any intervention.

From a bird's eye view, the application board only needs to host the connector to the DWAM78, a microcontroller for configuration of the DWAM78 and user controls (if desired) and an audio CODEC:



Pin List DWAM78

The host interface is a 30 pin 0.5mm pitch FFC (type number FCI SFV30R-4STE1, Molex 54104 3096 or equivalent). The pin functions are listed in the table below:

	Pin Number	Pin Name	I/O	Description
Audio	6	SDOUT_A	Bidirectional	I2S or S/P-DIF Out (port A)
	7	SDIN_A	In	I2S or S/P-DIF In (port A)
	8	BCK	Bidirectional	Bit Clock for ports A and B
	9	LRCK	Bidirectional	Left Right Clock for ports A and B
	14	AUDIO_CLK	Input	11.2896 MHz /12.288 TTL input
	10	SDOUT_B	Bidirectional	I2S output data, port B
	11	SDIN_B	Input	I2S input data, port B
Control	15	A0	Input	A0 and A1 form two bit offset address for 2-wire I2C Slave Address (Base Address 0x80)
	16	A1	Input	See A0
	17	I2C_SDA	Bidirectional	Data pin of 2 wire serial bus
	18	I2C_SCL	Output	Clock pin of 2wire serial bus
	19	INT	Output	Low Level Interrupt pin. Requires external pull-up resistor.
	20	RESN	Input	Low Active Reset Pin
	21	CTRL_SYNC	Bidirectional	Synchronization pin for CUIs (only applicable when operating collocated multiple CUIs)
	22	EN	Input	Enabling Wireless operation mode (no MCU)
	23	SYNC_STATUS	Output	Signal showing if module is in sync.
Power	1,2	VDD		3.3V Regulated voltage
	3,4,5	GND		
Miscellaneous	12, 13, 24, 25, 26, 27, 28, 30	NC		Leave Not Connected or connect to GND for isolation purposes.
	29	Debug_TXD		For debugging purposes

RF Connections

The MAX2 module has three Radial UMP R107.103.030 RF connectors. These can be configured as follows:

- One RF connection to an external antenna (no RX diversity, shared antenna for both TX and RX)
- Connection of two external antennas (RX diversity, one RX antenna is used for transmission)
- Connection of three external RF connectors (RX diversity and one dedicated TX antenna).

I2S bus

For mono or stereo applications, only the I2S port A (pins 6 and 7) has to be used. For three channel operation, I2S port B (pins 10 and 11) has to be used as well. The I2S bus BCK and LRCK signals (pins 8 respectively 9) are shared between ports A and B.

The audio clock at pin 14 (12.288MHz for 48ksps applications or 11.2896MHz for 44.1ksps applications) needs to be supplied from the application board (e.g. crystal oscillator).

I2C bus

The I2C bus (I2C_SDA and I2C_SCL at pins 17 and 18) accepts data rates up to 400kbps. The I2C base address is 0x80 and can be offset by setting pins A0 and A1 (pins 15 and 16). The I2C address is set at 0x80+A10.

The I2C bus can be connected to the I2C bus of the application's microcontroller or to its GPIO pins (the application software must then run the I2C protocol software).



Simple Stereo Application

For a simple stereo application, not all pins need to be used on the application board.

CTRL_SYNC (pin 21) is only used when you want to interconnect multiple CU's. EN (pin 22) is a HW enable pin, but it is advised that you enable/disable the module through register settings (through the I2C control interface), in which case EN must be connected to GND. SYNC_STATUS (pin 23) is a bit indicating if the wireless link is synchronized. This is also available through register settings (advised), so this pin may be left open.

In short, for a simple wireless stereo application, you would need to connect:

Pin1,2: VDD

Pin3,4,5: GND

Pin6,7,8,9: I2S interface

Pin14: audio clock (12.288MHz for 48ksps or 11.2896MHz for 44.1ksps)

Pin15,16: these may be hardwired to ground

Pin17,18,19: I2C with interrupt (interrupt requires external pull up resistor)

Pin22: EN may be hardwired to ground

All other pins may be ignored.

EMC

This chapter briefly addresses some common issues when designing and laying out the application board.

EMC test reports are available from the website for reference.

Power Supply

The DWAM78 accepts a 3.3V regulated supply voltage, capable of supplying peak currents of 250mA (for a few hundreds of μ s). If the application's power supply cannot deliver this peak current, then a buffer capacitor needs to be placed near the FFC to the DWAM78 to supply this peak current.

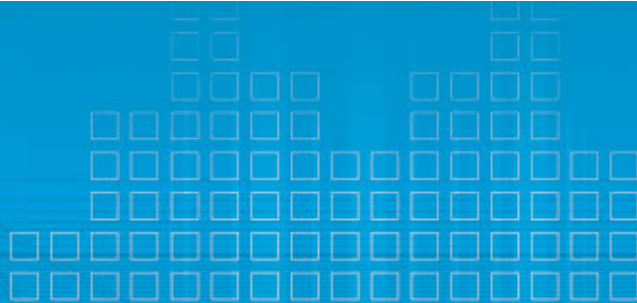
The DWAM78 frame repetition rate is in the order of 1kHz. The DWAM78 current draw is not constant during a frame period; depending on the application, the difference between minimum and maximum current in a frame period can range from about 100mA to 200mA. Therefore, care must be taken so that the varying current draw doesn't compromise power supply integrity of the analog audio circuitry on the application board. Separate regulators for the analog circuitry and DWAM78 may be considered, or simple Power Domain separation by means of beads/resistors and decoupling capacitors.

In general, it is advised that all ground connections of the application board are one solid ground plane (e.g. layer two of the PCB).

Audio Clock filtering

The audio clock signal runs over the flat foil cable to the DWAM78. The harmonics can easily radiate and exceed the regulatory limits if the drive strength is too strong and/or cable and/or PCB trace lengths are too long. To overcome this, the audio clock signal can be filtered at the source (i.e. at the crystal oscillator itself) by a simple filtering circuit such as depicted here below:



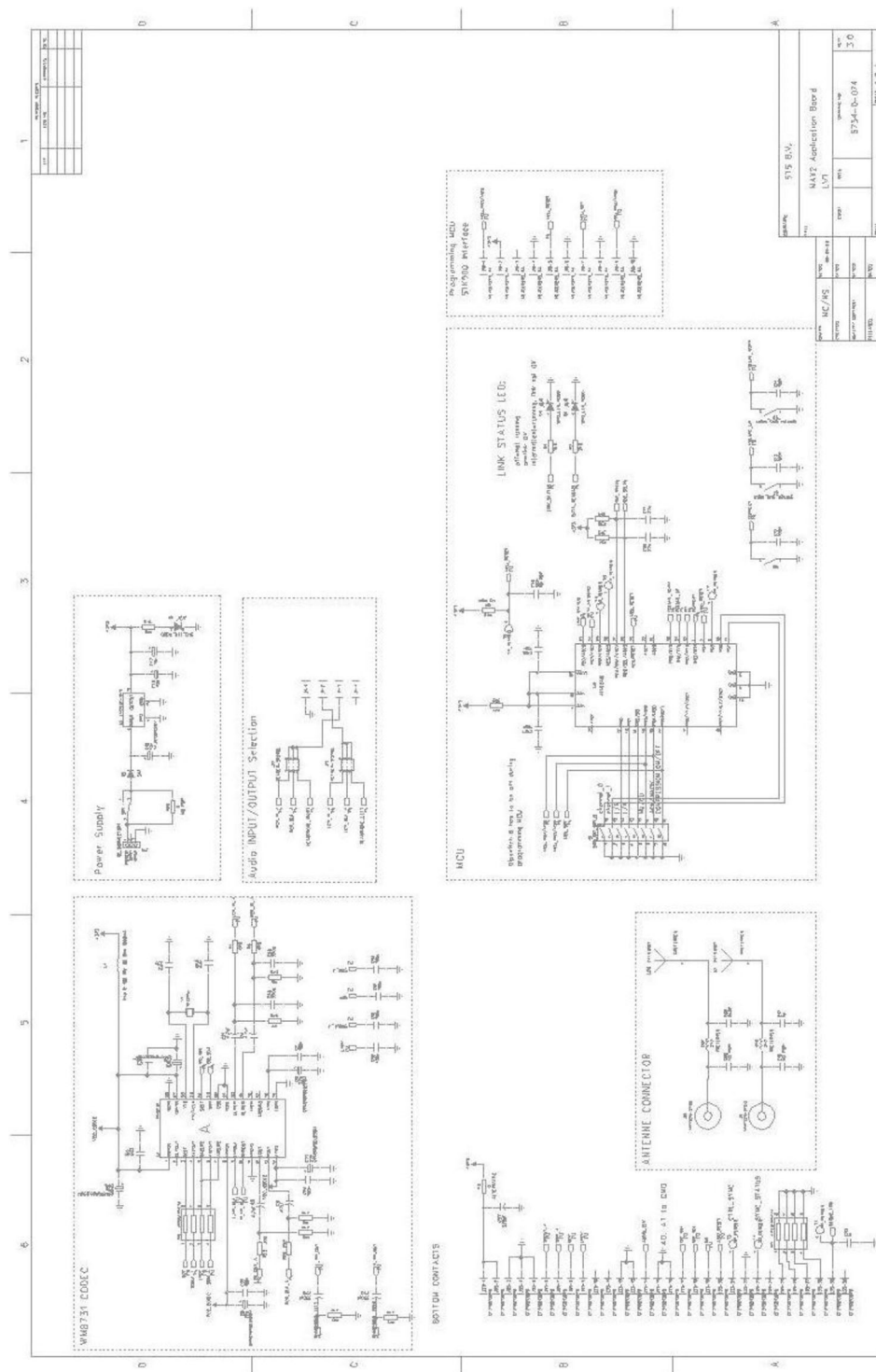


I2S Bus

The same (see “Audio Clock filtering”) holds for the I2S bus. It is advised that the bus is filtered on the application board with a resistor array (33...68Ohm) and small valued (e.g. 10pF) capacitors.

LVT Schematic

For the reader's reference, please find here below the schematic of the STS' LVT Application Board:



Please note that STS can also be your antenna partner.



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